REMARKS

At the outset, Applicants note with appreciation the Examiner's allowance of claims 17-20 and 24-29, and his indication of allowable subject matter in claims 1, 3, 5-7, 9, 10, 12-14, 22 and 23. It is respectfully requested that rewriting these dependent claims into independent form be held in abeyance in light of the remarks that follow. Claims 1-29 are currently pending.

The Office Action includes objections to the drawings and the Abstract. Changes are proposed to the drawings and abstract to accommodate the concerns expressed in the Office Action. It is respectfully submitted that these changes should be entered because they merely address informalities and further serve to simplify the issues. In light of these changes, withdrawal of these objections is respectfully requested.

The most recent Office Action maintained the rejections of independent claims 1, 4, 8, 11, 15, and 21 over either Cimini et al. (U.S. Patent No. 5,914,933) alone or a combination of this document with Daffara et al. (U.S. Patent No. 5,687,165). Reconsideration and withdrawal of these rejections are respectfully requested.

With respect to the rejection of claims 1 and 8 under 35 U.S.C. §102(a), as allegedly being anticipated by Cimini et al., Applicants' responses of February 23, 2004, and May 3, 2004, pointed out that the October 23, 2003 Office Action failed to point out how the apparatus of Cimini et al. meets the steps (b), (c) and (d) in claim 1. In the most recent Office Action, the Examiner asserts the following in sections 2 and 3 of the "Response to Arguments" section:

> Cimini discloses taking a serial data stream and breaking it into N symbol segments in ref. 119 ... These N symbol blocks are then converted into a parallel stream in ref. 31 .... Cimini discloses that the parallel signals (L small blocks) are passed through a FFT unit (ref. 41).

It is respectfully submitted, however, that the serial-to-parallel converter 31 of Cimini et al. converts a serial stream of N symbols, N being from 5 to 10 and respectively corresponding to 10- through 20-bit lengths (see column 11, lines 22-23), to *one word*. This one-word output from the converter 31 is then used as an input to a non-linear coder (i.e., a PAP-ROM) to look up and output a word that includes a number of bits having additional bits corresponding to an additional tone (e.g. a 14-bit PAP ROM output for a 12-bit input). The non-linear PAP coder output word is to be mapped to one more complex tone than normally would be mapped from the output from the converter 31 (e.g., a 14-bit word output from the PAP ROM will be mapped to seven tones instead of mapping the 12-bit output of the converter 31 to six tones). Hence, to the extent that the serial-to-parallel converter 31 of Cimini et al. could be considered to divide the N symbols into small blocks, it appears that each small block would be a size of *one* sample and the number of blocks would depend on the number of symbols in N. The original N symbols of Cimini et al. (e.g., comprising 12-bits), therefore, does not equal to the product of the small block size (i.e., 1) and number of the small blocks (i.e., 14). Hence, the relied upon disclosure of Cimini et al. does not disclose the claimed feature of "forming a block of N coded data and dividing the block into L M-sized small blocks, where N, M and L indicate integers of 1 or more, and L = N/M," as set forth in claim 1.

Additionally, the Cimini et al. patent does not disclose the claimed combination including the next recited feature of "(c) M-point inverse fast Fourier transforming the L small blocks." In contrast, the entire PAP coder output word of Cimini et al. is transformed using *only one* 56-point FFT. (See, column 5, equation (1) and lines 45-47.) The significance of this distinction is brought out in the next recited feature of "(d) combining L M-point inverse fast Fourier transformed blocks, and generating an N-sized inversely transformed block ...." By contrast, the logic device 45 of the Cimini et al. patent combines the output from separately addressed DFT ROMs 41a, 41b, which are addressed using groups of bits from the PAP ROM output (e.g., 7 bits each from the14-bit word output of the PAP ROMs), and outputs an 56 point block corresponding to *only one* FFT result. (See column 5, lines 45-47 and lines 56-57, and Figure 3.)

Hence, Cimini et al. does not show all the limitations recited independent claim 1, as pointed out above, and similar features recited in independent claim 8 with respect to an apparatus. Hence, claims 1 and 8 are considered allowable.

With respect to the rejection of claims 4 and 11 under 35 U.S.C. §103(a), as allegedly being unpatentable over Cimini et al. in view of Daffara et al., page 3 of the Action includes a statement that the Examiner does not consider Applicants' arguments set forth on pages 28 to 29 of the response convincing. More particularly, the Examiner states that because Cimini et al. "does teach the limitations of the claimed invention, given the above arguments." (See page 3, section 5.) However, for at least the reasons pointed out above, the method and apparatus for transmitting OFDM signals of Cimini et al. is fundamentally different from the Applicants' claimed

invention. Thus, even if the reverse process in the receiver could be considered obvious in view of transmitter process, the processes (c), (d) and (e) in claim 4 and the recitation of, "a signal receiving deinterleaver for dividing ...; a signal receiving interleaver for interleaving the L M-point fast Fourier transformed small block, thereby generating an N-sized transform block," in claim 11, lines 6-11, are not taught or suggested by the combination of Cimini et al. and Daffara.

For at least these reasons, the rejection of independent claims 4 and 11 should be withdrawn.

On pages 9-11, the Office Action maintained the rejection of Claims 15, 16 and 21 under 35 U.S.C. §103(a), as allegedly being unpatentable over Cimini et al. Applicants' responses of February 23, 2004, and May 3, 2004, however, pointed out a number of differences from the claims and the method and apparatus described in the Cimini et al. patent. Specifically with respect to claim 15, Applicants traversed the suggestion in the Office Action that Cimini et al. shows all the limitations recited claims 15, 16 and 21 except for inserting "0" at the first position of each block after dividing the encoded data into blocks of predetermined sizes (see, for example, Applicants' response of May 3, 2004, pages 29-31). The following analysis of the claims points out these differences in greater detail.

Claim 15 is directed to an apparatus for transmitting OFDM signals that comprises, among other features, a pre-processor for encoding an input data sequence and converting the encoded data to parallel data. In connection with this feature, on page 3, section 6 of the Action, the Examiner alleges that the combination of the encoder 21 and demultiplexer circuit 26 of Cimini et al. can be

viewed as the claimed pre-processor. The next recited feature of claim 15 is "a block signal domain transformer" for:

> dividing the encoded data into blocks of predetermined sizes,
>
> inserting "0" at the first data position of each block,
>
> transforming each block into a time domain signal, and
>
> combining time domain signals.

That is, the block signal domain transformer operates to divide "the encoded data," which is the recited encoded data converted to parallel data, into blocks of predetermined sizes. On page 4, section 7 of the Office Action, the Examiner asserts this feature to be disclosed by the S/P converter 31 of Cimini et al. However, the S/P converter 31 does not operate to divide "the encoded data" as recited in the context of claim 15. Rather, it operates on *only one* "M block" of the encoded parallel data on one of the separate M subchannels. (See, column 3, lines 2-8.) Hence, even if one were to consider, for the sake of argument, that the combination of the encoder 21 and the demultiplexer 26 to correspond to a "pre-processor," the S/P converter 31 of Cimini et al. does not operate to divide "the encoded data" as claimed.

Furthermore, the S/P converter 31 of Cimini et al. does not operate to divide the N symbol signal data 25a into blocks of predetermined sizes as claimed. As pointed out above, the converter 31 produces *only one* parallel 12-bit (or 14-bit) word from these data.

With respect to the claimed features of transforming each block into a time domain signal and combining time domain signals, the Examiner asserts that

the P/S converter 45 of Cimini et al. "combines the parallel time-domain signals into a single serial time-domain signal." (See, page 4, lines 6-9.) It is respectfully submitted, however, that the P/S converter of Cimini et al. does not operate to combine time domain signals as claimed. According to Cimini et al., a single word (e.g., a 12-bit or 14-bit word) produced by the serial-to-parallel converter 31 is input to a PAP ROM, which outputs a coded word 39 including additional bits (e.g., 14- or 16-bits). The coded word 39 addresses the DFT ROMs 41a, 41b to produce 8-bit DFT representations, which are then added together in the programmable logic device (PLD) 45, for 64 samples to produce *one* time domain signal (e.g., a 7- or 8-tone signal). (See column 6, lines 9-28, column 4, lines 28-31, and Figure 3.) Hence, the PLD 45 of Cimini et al. does not combine transformed time domain *signals* as claimed because it outputs only one time domain signal.

With respect to the claimed feature of the block signal domain transformer "inserting "0" at the first data position of each block," the Examiner acknowledges this feature not to be disclosed in the Cimini et al. patent, but he continues to allege this feature would have been obvious in view of the teaching in Cimini et al. of storing a guard interval for each of the 64 samples stored in the DFT ROMs 41. However, considering the Examiner's arguments that allege the DFT of Cimini et al. to actually be IFFT (see, section 3 spanning pages 2-3), the stored samples in the DFT ROMs 41 would represent time domain signals. As such, any such guard interval is stored with the *resultant* IFDT *time domain* values and does not relate to claimed feature of "inserting "0" at the first position of each block" and "transforming each block into a time domain signal ...," as recited in claim 15.

Moreover, Applicants' reiterate their disagreement with the Examiner's allegation that inserting "0" at the first position of each block would have been obvious in view of disclosure in Cimini et al. of use of a guard interval and in absence of criticality (Office Action, page 8, first paragraph). As pointed out above, the guard interval described in Cimini et al. is stored in a DFT ROM 41, which the Examiner alleges to be an IFFT. Therefore, the lack of any teaching or suggestion in Cimini et al. of inserting "0" into positions of each of pre-transformed blocks is further evidence of the nonobviousness of the present invention, which inserts "0" at the first data position of each block, for instance, to avoid DC offset (page 16, lines 1-2). As pointed out in Applicants' previous responses, inserting "0" as claimed has nothing to do with a guard interval. Guard intervals are designed to prevent intersymbol interference. The present invention adopts cyclic prefixes as a guard interval, which is additional evidence that the guard interval of Cimini et al. is not the same as inserting "0s" as recited in the claims.

Applicants' responses also pointed out that Cimini et al. fails to teach or suggest the claimed features of "a pilot signal adder for converting pilot tones, which are to be inserted at positions other than a predetermined position among the positions at which "0" has been inserted in the block signal domain transformer, into time domain pilot signals, and adding the pilot signals to the time domain signals output by the block signal domain transformer." In response, the Office Action states "that the pilot tones are used for the same reason as [Applicants'] claimed invention," is not recited in claim 15. However, when specifically addressing claim 15, Applicants' response identified other distinguishing features of the invention recited

in that claim. Specifically, the last paragraph of page 30 of the response contains the following statements:

> Furthermore, Cimini et al. does not show "a pilot signal adder for converting pilot tones, which are to be inserted at positions other than a predetermined position among the positions at which "0" has been inserted in the block signal domain transformer, into time domain pilot signals, and adding the pilot signals to the time domain signals output by the block signal domain transformer" as recited in claim 15 and step (d) in claim 21. The Office indicated that transforming pilot tones is taught by Cimini et al. (see Office Action, page 7, paragraph 17). However, it is respectfully submitted that Cimini et al. does not teach where the pilot tones are to be inserted, or the pilot tones are used for the same reason as the Applicants claim invention.

The most recent Office Action does not address these points of distinction that were brought out by Applicants. For instance, the portions of Cimini et al. relied upon by the Examiner (i.e., column 4, lines 40-50 and column 7, line 65 to column 8, line 14) are silent with regard to how pilot signals are prepared and sent over each of the clusters 27a to 27M of Cimini et al. As such, there cannot be any teaching or suggestion in Cimini et al. of the parallel-to-serial converter (PLD) 45 that operates to "convert pilot tones, which are to be inserted at positions other than a predetermined position among the positions at which '0' has been inserted in the block signal domain transformer, into time domain signals, and adding the pilot signals to the time domain signals output by the block signal domain transformer ...," as set forth in claim 15, and similarly recited in processes of claim 21.

Claim 15 also recites, *inter alia*, a post-processor for converting the *resultant signals* of the pilot signal adder to serial signals. These *resultant signals* of the pilot signal adder, in turn, are formed using "time domain signals *output by the block signal domain transformer.*" (See claim 15, lines 10-12.) In this regard, it is noted

that the Examiner has not addressed Applicants' argument that the parallel-to-serial converter (PLD) 45 cannot be asserted to function as both "combining the time domain signals" (see Office Action, page 7, line 12) and "converting the resultant signals of the pilot signal adder to serial signals."

Furthermore, Applicants disagree with the statements in the Office Action on page 5, section 10, concerning Cimini's alleged disclosure of a pilot tone being added to the output from the cluster. With respect to transmitting pilot tones, the cited disclosure in Cimini et al. only mentions that "pilot tones are sent over each cluster 27a, ... , 27M and, at the expense of receiver training, the receiver measures the frequency response of each subchannel associated with each of the clusters." (See, column 8, lines 2-5.) There is simply no teaching or suggestion in Cimini et al. that such pilot tones are inserted "at positions other than a predetermined position among the positions at which '0' has been inserted in the block signal domain transformer," as claimed.

Additionally, the recited post-processor in claim 15 operates to add a cyclic prefix to each of the converted signals. The Action asserts that this feature is disclosed in Cimini et al., at column 5, line 56 to column 5, line 8. (See, page 10, line 11.) However, according to the portion of Cimini et al. the Examiner relies upon, the ROM lookup table 41 performs cyclic prefixing (column 5, line 67 to column 6, line 2). Because the Examiner has asserted element 41 in Cimini et al. functions as a block signal domain transformer (page 4, lines 5-11), it cannot also function as the claimed "post-processor."

For at least these reasons, the Cimini et al. patent does not show all the recitations recited in claim 15 as the applicants have pointed out, above, and there is no motivation to alter Cimini et al. to meet these recitations. Claim 21 recites similar distinctions that are not taught or suggested in the Cimini et al. patent and is therefore allowable. Accordingly, the rejection of claims 15 and 21 should be withdrawn.

Because independent claims 1, 4, 8, 11, 15 and 21 are allowable, it is respectfully submitted that all claims dependent thereon are also allowable.

For the foregoing reasons, it is respectfully submitted that all pending claims are patentable over the disclosure of the Cimini et al. patent and any combination of this document with the Daffara et al. patent. If the rejection of any of the claims is maintained, the Examiner is requested to identify how that patent is being interpreted to suggest the specific distinguishing features discussed above. In the absence of such a showing, it is respectfully submitted that the rejection should be withdrawn.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

Date: September 15, 2004

By: _____
John F. Guay
Registration No. 47,248

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620

Attachment: Replacement Sheets (2)
Annotated Sheets Showing Changes (2)

FIG. 5

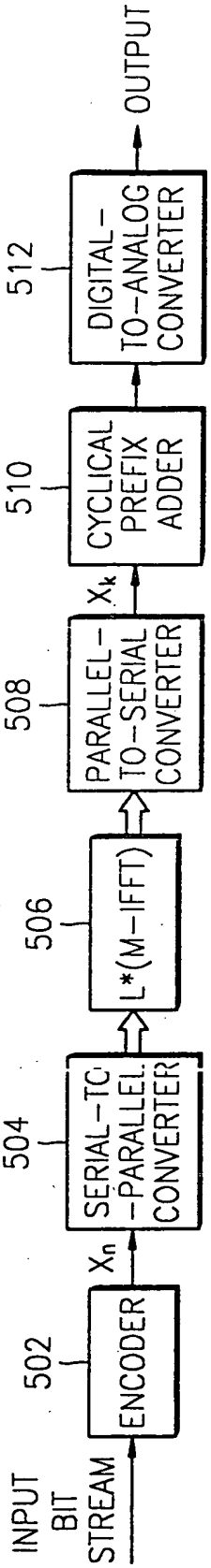
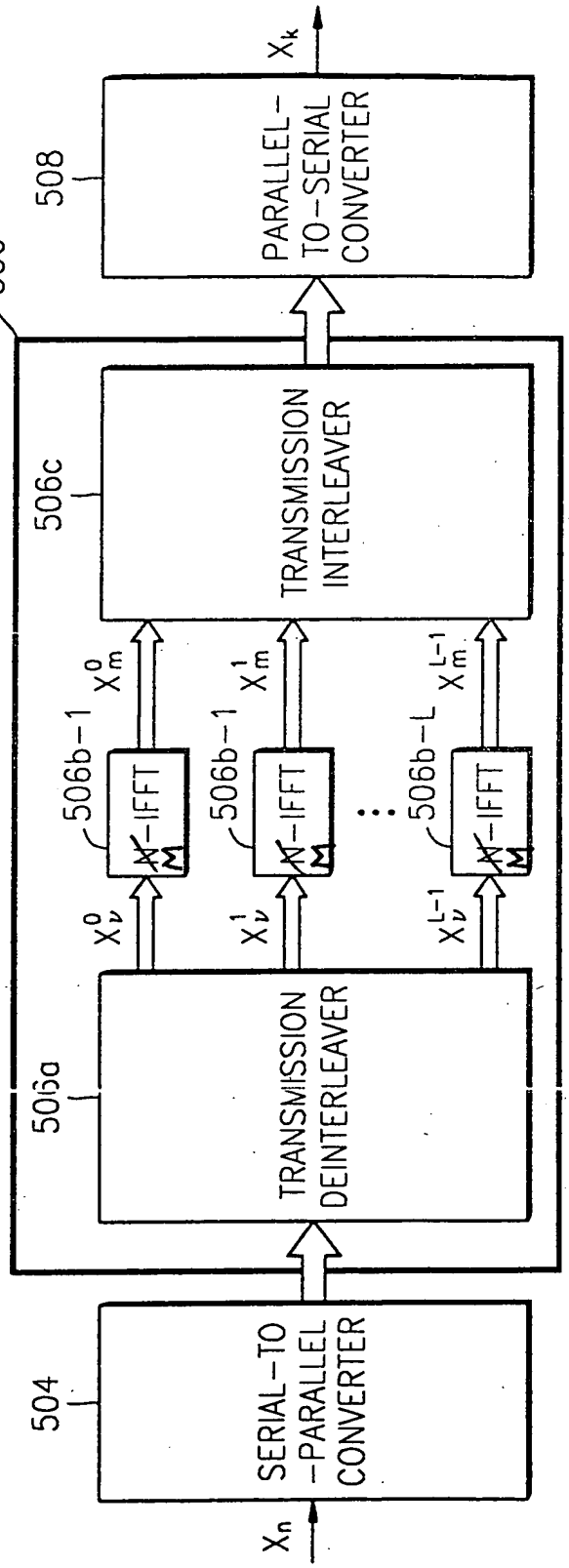


FIG. 6



Annotated Sheet

FIG. 16